FIG. 1

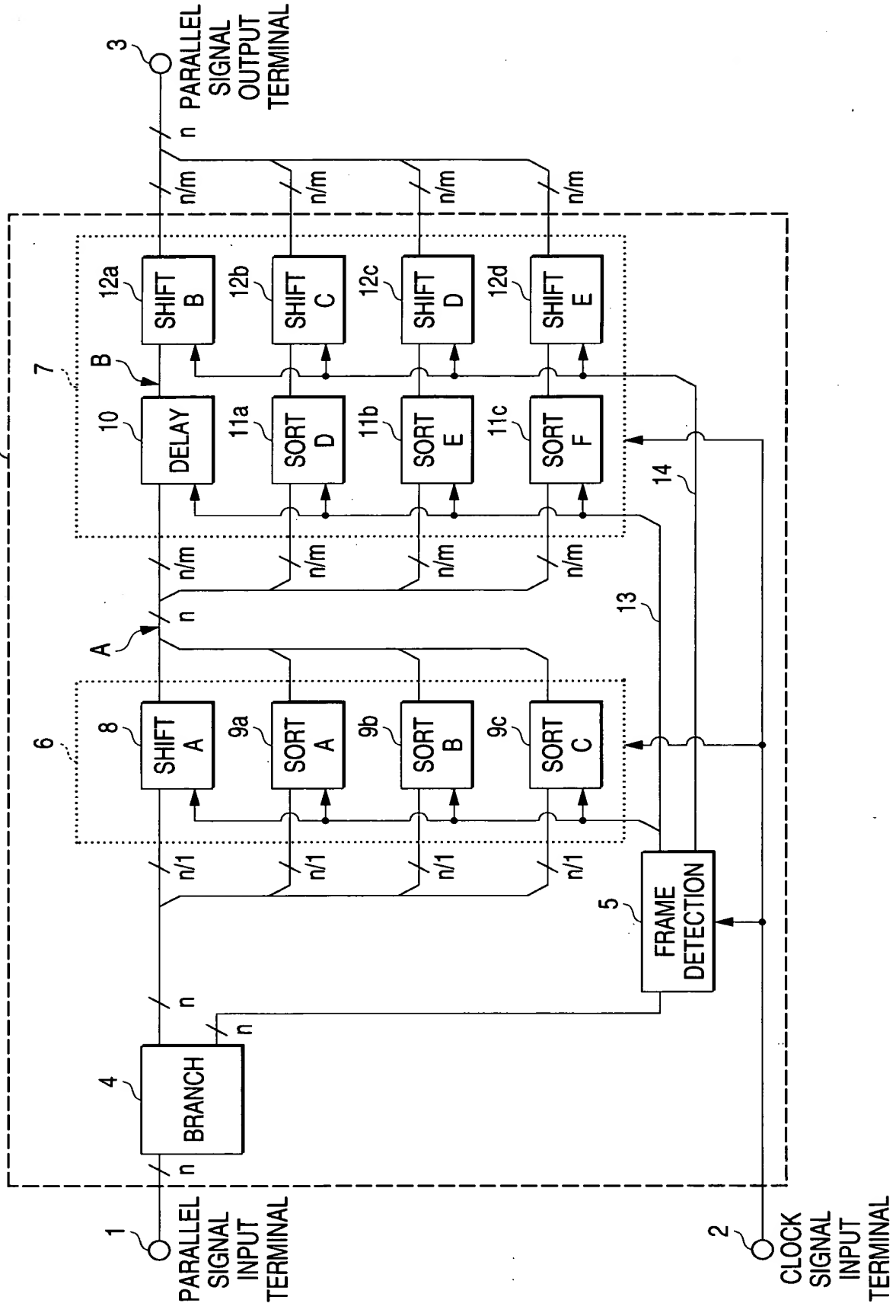

100
1
PARALLEL SIGNAL INPUT TERMINAL
2
CLOCK SIGNAL INPUT TERMINAL
3
PARALLEL SIGNAL OUTPUT TERMINAL
4
BRANCH
5
FRAME DETECTION
6
7
8
SHIFT A
9a
SORT A
9b
SORT B
9c
SORT C
10
DELAY
11a
SORT D
11b
SORT E
11c
SORT F
12a
SHIFT B
12b
SHIFT C
12c
SHIFT D
12d
SHIFT E
13
14
A
B
n
n/m
n/1

FIG. 2

TRUTH TABLE OF SHIFT CIRCUITS A TO E
(WHERE INPUT OF SORT CIRCUIT AND SHIFT CIRCUIT IS 4 BITS)

INPUT						OUTPUT			
D0	D1	D2	D3	SEL	CLK	Q0	Q1	Q2	Q3
A	B	C	D	0	↑	A	B	C	D
A	B	C	D	1	↑	B	C	D	A (+1)
A	B	C	D	2	↑	C	D	A (+1)	B (+1)
A	B	C	D	3	↑	D	A (+1)	B (+1)	C (+1)

FIG. 3

TRUTH TABLE OF SORT CIRCUITS A TO C
(WHERE INPUT OF SORT CIRCUIT IS 4 BITS)

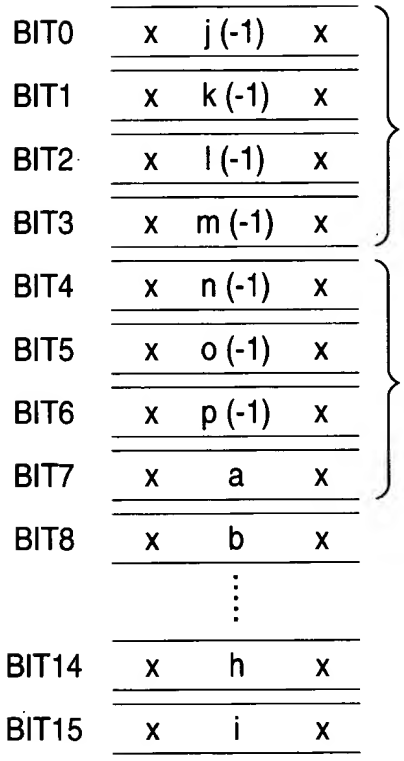
INPUT						OUTPUT			
D0	D1	D2	D3	SEL	CLK	Q0	Q1	Q2	Q3
A	B	C	D	0	↑	A	B	C	D
A	B	C	D	1	↑	B	C	D	A
A	B	C	D	2	↑	C	D	A	B
A	B	C	D	3	↑	D	A	B	C

FIG. 4

TRUTH TABLE OF SORT CIRCUITS D TO F IN ENABLE
(WHERE INPUT OF 1 BIT SHIFT CIRCUIT IS 4 BITS)

INPUT					OUTPUT			
D0	D1	D2	D3	CLK	Q0	Q1	Q2	Q3
A	B	C	D	↑	B	C	D	A

FIG. 5A



LOW ORDER BIT OF FRAME POSITION SIGNAL

FIG. 5B

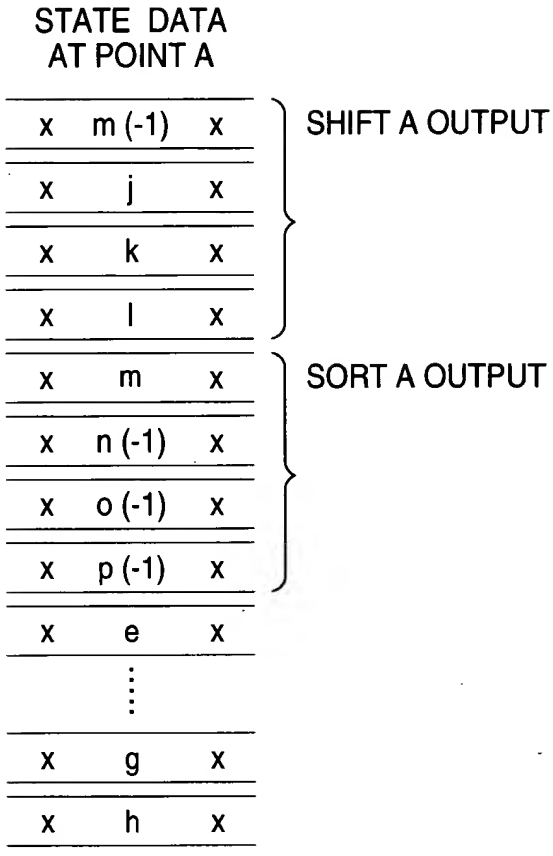


FIG. 6A

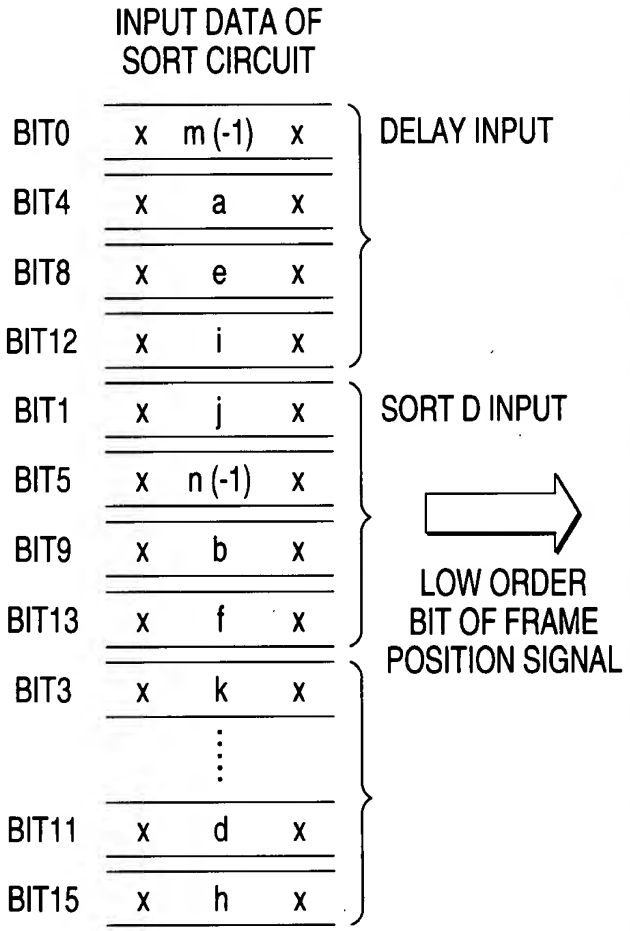


FIG. 6B

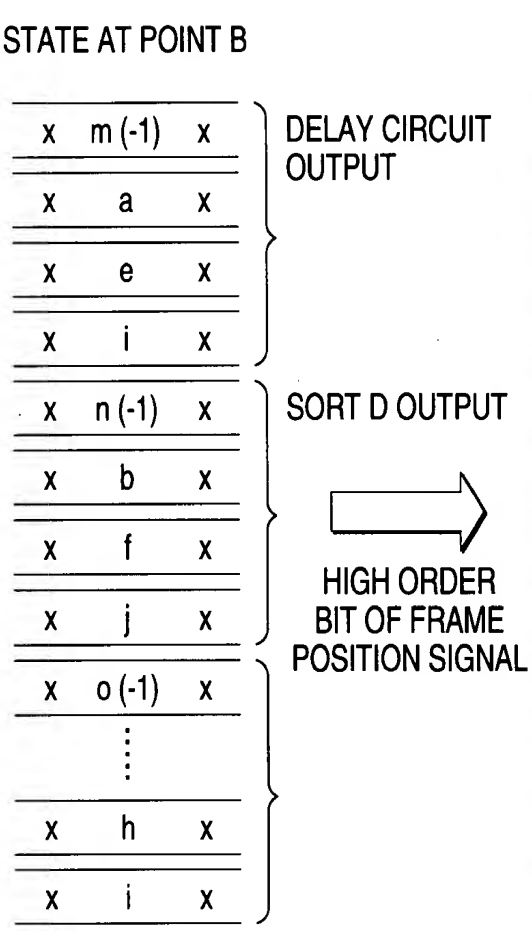


FIG. 6C

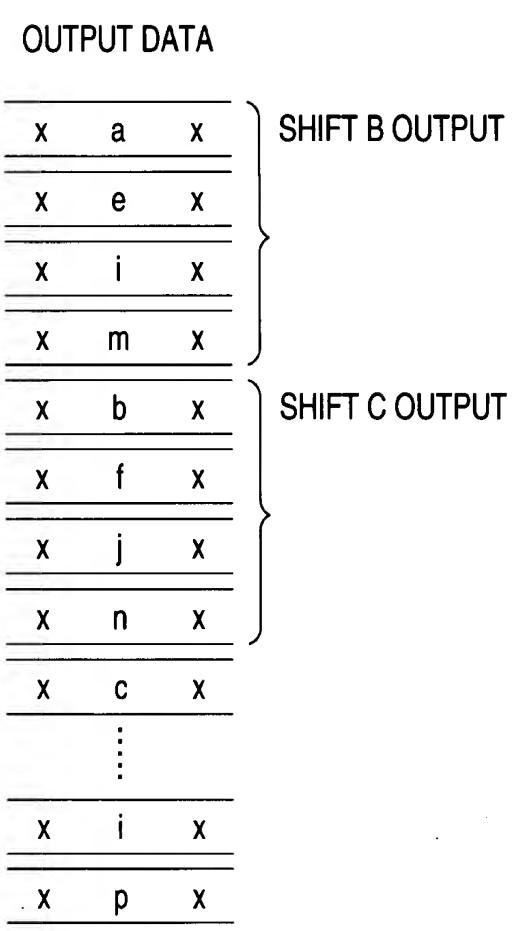


FIG. 7

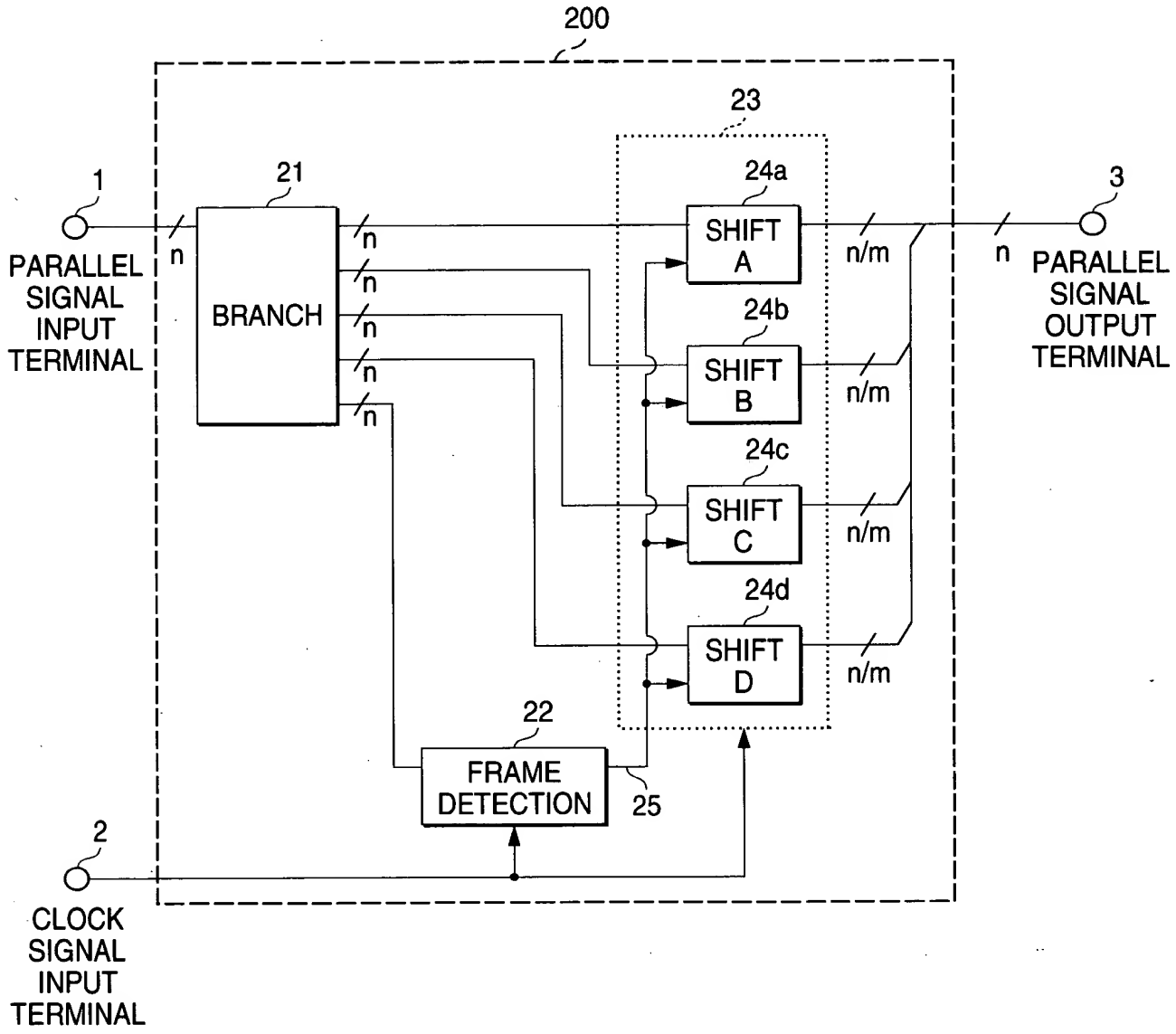

200
23
1
21
24a
3
PARALLEL SIGNAL INPUT TERMINAL
n
BRANCH
n
n
n
n
SHIFT A
n/m
n
PARALLEL SIGNAL OUTPUT TERMINAL
24b
SHIFT B
n/m
24c
SHIFT C
n/m
24d
SHIFT D
n/m
22
FRAME DETECTION
25
2
CLOCK SIGNAL INPUT TERMINAL

FIG. 8

TRUTH TABLE OF SHIFT CIRCUIT A
(WHERE DATA INPUT IS 16 BITS, AND THERE ARE FOUR SHIFT CIRCUITS)

INPUT							OUTPUT			
D0	D1	D2	···	D15	SEL	CLK	Q0	Q1	Q2	Q3
A	B	C	···	P	0	↑	A	B	C	D
A	B	C	···	P	1	↑	B	C	D	E
A	B	C	···	P	2	↑	C	D	E	F
A	B	C	···	P	···	↑	···	···	···	···
A	B	C	···	P	15	↑	P	A (+1)	B (+1)	C (+1)

FIG. 9

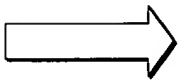
TRUTH TABLE OF SHIFT CIRCUIT B
(WHERE DATA INPUT IS 16 BITS, AND THERE ARE FOUR SHIFT CIRCUITS)

INPUT							OUTPUT			
D0	D1	D2	···	D15	SEL	CLK	Q0	Q1	Q2	Q3
A	B	C	···	P	0	↑	E	F	G	H
A	B	C	···	P	1	↑	F	C	H	I
A	B	C	···	P	2	↑	C	H	I	J
A	B	C	···	P	···	↑	···	···	···	···
A	B	C	···	P	15	↑	D (+1)	E (+1)	F (+1)	G (+1)

FIG. 10A

DATA INPUT

BIT0	x	j (-1)	x
BIT1	x	k (-1)	x
BIT2	x	l (-1)	x
BIT3	x	m (-1)	x
BIT4	x	n (-1)	x
BIT5	x	o (-1)	x
BIT6	x	p (-1)	x
BIT7	x	a	x
BIT8	x	b	x
		⋮	
BIT14	x	h	x
BIT15	x	i	x



FRAME
POSITION SIGNAL

FIG. 10B

DATA OUTPUT

x	a	x
x	b	x
x	c	x
x	d	x
x	e	x
x	f	x
x	g	x
x	h	x
x	i	x
	⋮	
x	o	x
x	p	x

SHIFT A OUTPUT

SHIFT B OUTPUT

FIG. 11

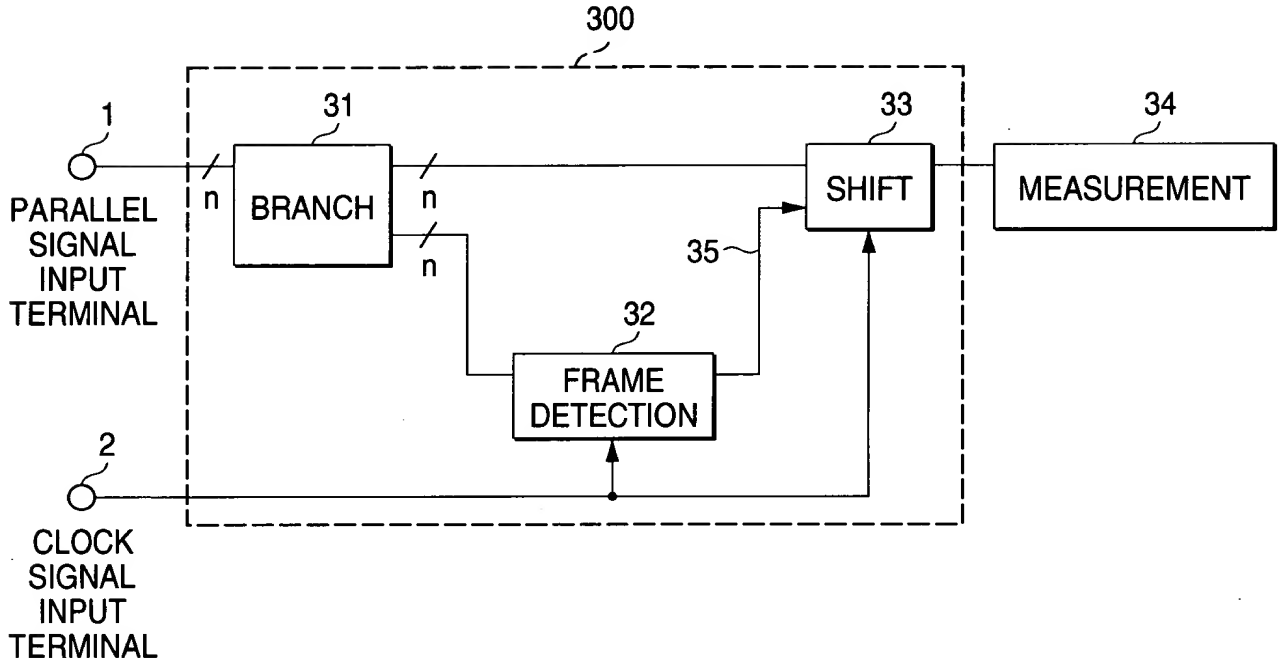


FIG. 12

TRUTH TABLE OF SHIFT CIRCUIT (WHERE DATA INPUT IS 16 BITS)

INPUT							OUTPUT				
D0	D1	D2	· · ·	D15	SEL	CLK	Q0	Q1	Q2	· · ·	Q3
A	B	C	· · ·	P	0	↑	A	B	C	· · ·	P
A	B	C	· · ·	P	1	↑	B	C	D	· · ·	A (+1)
A	B	C	· · ·	P	2	↑	C	D	E	· · ·	B (+1)
A	B	C	· · ·	P	· · ·	↑	· · ·	· · ·	· · ·	· · ·	· · ·
A	B	C	· · ·	P	15	↑	P	A (+1)	B (+1)	· · ·	O (+1)